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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/605,099	09/09/2003	Chih-Hung Wang	11555-US-PA	2098
31561	7590 08/03/2005		EXAM	INER
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE			FARROKH, HASHEM	
7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100			ART UNIT	PAPER NUMBER
			2187	
TAIWAN			DATE MAILED: 08/03/200	5

Please find below and/or attached an Office communication concerning this application or proceeding.

X · ·				
7)	Application No.	Applicant(s)		
	10/605,099	WANG, CHIH-HUNG		
Office Action Summary	Examiner	Art Unit		
	Hashem Farrokh	2187		
The MAILING DATE of this communic Period for Reply	ation appears on the cover sheet	with the correspondence address		
A SHORTENED STATUTORY PERIOD FO THE MAILING DATE OF THIS COMMUNIC  - Extensions of time may be available under the provisions or after SIX (6) MONTHS from the mailing date of this commu  - If the period for reply specified above is less than thirty (30)  - If NO period for reply is specified above, the maximum state  - Failure to reply within the set or extended period for reply w Any reply received by the Office later than three months after earned patent term adjustment. See 37 CFR 1.704(b).	CATION.  f 37 CFR 1.136(a). In no event, however, may nication.  days, a reply within the statutory minimum of the statutory period will apply and will expire SIX (6) Moreover than the statute, cause the application to become	a reply be timely filed  hirty (30) days will be considered timely.  DNTHS from the mailing date of this communication.  ABANDONED (35 U.S.C. § 133).		
Status				
1) Responsive to communication(s) filed	on 09 September 2003.			
	n)⊠ This action is non-final.			
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.				
Disposition of Claims				
4) ⊠ Claim(s) 1-10 is/are pending in the ap 4a) Of the above claim(s) is/are 5) ⊠ Claim(s) 4 and 6-8 is/are allowed. 6) ⊠ Claim(s) 1-3,5,9-10 is/are rejected. 7) □ Claim(s) is/are objected to. 8) □ Claim(s) are subject to restrictions.	e withdrawn from consideration.			
Application Papers	·			
9)☐ The specification is objected to by the	Evaminer			
10) The drawing(s) filed on is/are:		o by the Examiner.		
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).				
	he correction is required if the drawir	ng(s) is objected to. See 37 CFR 1.121(d).		
Priority under 35 U.S.C. § 119				
12) Acknowledgment is made of a claim for a) All b) Some * c) None of:  1. Certified copies of the priority of the priority of the certified copies of the priority of the certified copies of the certified copies of application from the Internation * See the attached detailed Office action	ocuments have been received. ocuments have been received in f the priority documents have bee al Bureau (PCT Rule 17.2(a)).	Application No en received in this National Stage		
Attachment(s)	»□			
<ol> <li>Notice of References Cited (PTO-892)</li> <li>Notice of Draftsperson's Patent Drawing Review (PT 3)</li> <li>Information Disclosure Statement(s) (PTO-1449 or P Paper No(s)/Mail Date</li> </ol>	O-948) Paper N	v Summary (PTO-413) o(s)/Mail Date f Informal Patent Application (PTO-152) 		
U.S. Patent and Trademark Office PTOL-326 (Rev. 1-04)	Office Action Summary	Part of Paper No./Mail Date 20050730		

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The instant application having application No. 10/605,099 has a total of 10 claims pending in the application; there are 2 independent claims and 8 dependent claims, all of which are ready for examination by the examiner.

#### INFORMATION CONCERNING CLAIMS:

## Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 5, and 9-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- 1. In regard to claim 1, the expression "a plurality of sector by N" makes this claim indefinite because of grammatical and idiomatic errors. The examiner would suggest to replace "a plurality of sector by N" with "a plurality of sectors).
- 2. In regard to claim 5, the expression a command "15H" makes this claim indefinite, since it is difficult to understand the metes of the claim.
- 3. In regard to claim 9, the expression <u>a "10H" command</u> makes this claim indefinite, since it is difficult to understand the metes of the claim.
- 4. In regard to claim 10, the expression <u>a "15H" command</u> makes this claim indefinite, since it is difficult to understand the metes of the claim.

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## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6871,257 B2 to Conley et al. (hereinafter Conley).

5. In regard to claim 1, Conley teaches:

"An accessing method to a large block flash memory (e.g., see column 1, line 10, elements 131 in Fig. 2) of a memory device, (e.g., see column 1, lines 30-34) wherein the large block flash memory has a plurality of pages (e.g., see column 1, line 44) and each page has a plurality of sectors by N, (e.g., see column 1, line 46) wherein the memory device has a controller to control an access operation between a host and the large block memory of the memory device, (e.g., see column 3, lines 62-67; column 4, lines 1-1-4; elements 101 and 131 in Fig. 2) wherein the controller includes at least two buffers, (e.g., see column 7, lines 26-30, elements 111A-111B in Fig. 3) when the host intends to program the memory device, (e.g., see column 7, lines 26-30) the method comprising:"

"transferring data sectors between the host and the large block flash memory by alternatively using the buffers;" (e.g., see column 8, lines 1-32; elements 111A-111B, 131-0 AND 131-1

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in Fig. 2). The host transfers a set of data to BUFA and controller transfer this data to Flash memory. While the controller is writing this data to memory, the host transfer a second set of data to BUFB. After transfer of data from BUFA to memory is complete, the controller transfer the data from BUFB to memory and the host write the third set of data to BUFA. Thus transfer of data between the host and the Flash memory takes place by alternatively using the buffers. "and issuing a start program command by the controller for programming the large block flash memory after transferring N data sectors with respect to one page." (e.g., see column 8, lines 51-60; Fig. 4a-4b). For example after transfer of data to BUFA (prior to time t), the controller transfer the data to the memory and begin programming (e.g., issuing a start program command) the Flash memory.

6. In regard to claim 2, Conley teaches:

"wherein the at least two buffers have two buffers, (e.g., see column 8, lines 1-32; elements 111A-111B) and the step of transferring data between the host and the large block flash memory comprises:" (e.g., see column 8, lines 51-60). Conley teaches that the buffer is being loaded with pages which inherently consists of a plurality smaller buffers.

"alternatively using one of the two buffers to store a data transferred from the host;" (e.g., see column 8, lines 1-32).

"transferring a previous data stored in the other one of the two buffers to the large block flash memory;" (e.g., see column 8, lines 1-14). After completing transfer of data from BUFA, controller transfer the content of BUFB which is already transferred from the host. This data is considered previous data.

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"and calculating an address for the data to be programmed to the large block flash memory by the controller, (e.g., see column 1, lines 50-56) wherein at least two of the above three different operations can be performed at the same time." (e.g., see column 8, lines 1-7). For example translation of Logical Block Address (LBA) to Logical Block Number (LBN) represents calculating address recited in the claim. Transfer of data from the host to one of the buffer in the controller and the programming of the Flash memory are performed at the same time.

## 7. In regard to claim 3, Conley teaches:

"wherein the large block flash memory further includes two buffers, (e.g., see column 8, lines 1-14) and the method further comprises:"

"sending a page of data from the controller to a data cache within the large block flash memory;" (e.g., see column 8, lines 11-14 and 55-56; element 135-0 and 135-1 in Fig. 3).

For example the registers 135-0 and 135-1 in Fig. 3 represent the data cache recited in the claim.

"after the data cache is full, shifting a data content in the data cache to a page buffer within the large block flash memory;" (e.g., see column 8, lines 51-60; Figs. 4a-4b). The data stored in REG0 is programmed in sectors of Flash memory (e.g., MEM0).

"and continuously sending a next page of data to the data cache while a content in the page buffer is programmed to a cell array of the large block flash memory." (e.g., see column 5, lines 42-52).

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ALLOWABLE SUBJECT MATTER

Claims 4 and 6-8 are allowed.

1. The primary reason for allowance of claims 4 and 6-8 in instant application is

the combination with the inclusion of the following limitation: **shifting the current** 

page data in the data cache to the a page buffer within the large block flash

memory.

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: <u>IMPORTANT NOTE</u> :

If the applicant should choose to rewrite the independent claims to include

the limitations recited in either one of the claims, the applicant is encouraged to

amend the title of the invention such that it is descriptive of the invention as

claimed as required be sec. 606.01 of the MPEP. Furthermore, the summary of

invention and the abstract should be amended to bring them into harmony with

the allowed claims as required by paragraph 2 of sec. 1302.01 of the MPEP.

As allowable subject matter has been indicated, applicant's response must

either comply with all formal requirements or specifically traverse each

requirement not compiled with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the

M.P.E.P.

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#### Conclusion

The prior art made of record and not relied upon are as follows:

- 1. U. S. Patent No. 6,317,371 to Katayama et al. describes Storage device with an error correction unit and an improved arrangement for accessing and transferring blocks of data stored in a non-volatile semiconductor memory.
- 2. U. S. Patent No. 6,405,279 to Kondo et al. describes Apparatus and method for controlling rewriting of data into nonvolatile memory.
- 3. U. S. Patent No. 5,701,516 to Cheng et al. describes High-performance non-volatile RAM protected write cache accelerator system employing DMA and data transferring scheme.
- 4. U. S. Patent No. 6,684,289 to Gonzalez et al. describes Techniques for operating non-volatile memory systems with data sectors having different sizes than the sizes of the pages and/or blocks of the memory.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from 8:00 AM to 5:00 PM.

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or

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2005-07-30

NASSER MOAZZAMI PRIMARY EXAMINER